REMARKS/ARGUMENT

In the most recent Office Action, claims 1-19 were examined. Claims 1-19 are rejected. Claims 1, 7-8 and 16 are amended. Accordingly, claims 1-19 are pending in the present application. No new matter is added.

Applicants thank the Examiner for the thorough search and examination in the present Office Action, and respond to the comments in the Office Action as follows.

Claim Rejections - 35 U.S.C. §103

Claims 16-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Miyasaka (U.S. Patent No. 6,124,154). In particular, the Office Action states that Miyasaka shows the invention as claimed and, apparently in combination with the disclosure by Yamazaki (U.S. Patent No. 6,306,213), shows the specific ranges claimed. The rejection is respectfully traversed.

The Office Action states that the disclosure by Miyasaka lacks anticipation of the processing conditions with respect to the polysilicon layer and the thermal oxidation and densification processes. That is, Miyasaka fails to show:

> thermally depositing a silicon oxide gate dielectric layer on said polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700 Angstroms,

as is recited in claim 16. The Office Action apparently seeks to obtain this element from the disclosure by Yamazaki. However, both the disclosures by Miyasaka and Yamazaki make clear that the disclosed structures are not composed of a polysilicon layer underneath the silicon oxide gate dielectric layer. Miyasaka notes that the semiconductor layer underneath the silicon oxide gate dielectric layer is crystallized prior to deposition of the silicon oxide layer, to produce a smooth single crystalline semiconductor layer (col. 16, line 30-col. 17, line 15). Yamazaki shows the semiconductor layer underneath the gate dielectric layer is crystallized to produce a higher carrier mobility than that of polycrystalline silicon, prior to the deposition of a gate dielectric layer (col. 7, line 17-col. 8, line 17). Accordingly, neither of the disclosures by

Miyasaka or Yamazaki teach or suggest the process performing a thin film transistor device according to claim 16:

> forming a rough polysilicon layer on said insulating substrate;
>
> thermally depositing a silicon oxide gate dielectric layer on said polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700 Angstroms; and
>
> performing an anneal procedure to densify said silicon oxide gate dielectric layer.

In each of the references by Miyasaka and Yamazaki, a gate dielectric layer is deposited upon a crystallized semiconductor layer, rather than a polysilicon layer, as is recited in claim 16. As stated in the previous response, polysilicon has a much rougher surface texture than crystallized silicon, and becomes even rougher when annealed (the size of the grains increases). Accordingly, the features of the present invention are not realized in the cited prior art references. Accordingly, claim 16 recites elements that are not taught or suggested in the cited prior art references, either alone or in combination. Claim 16 is therefore thought to be allowable under 35 U.S.C. §103(a) over the disclosures by Miyasaka and Yamazaki, and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Claims 17-19 depend upon and further limit claim 16, and should be allowable for the same reasons as claim 16, and additionally for the further limitations recited in each dependent claim. Accordingly, Applicants respectfully request that the rejection of claims 17-19 under 35 U.S.C. §103(a) be reconsidered and withdrawn

Claims 1-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. (U.S. Patent No. 6,037,199) in view of Doklan et al. (U.S. Patent No. 4,851,370). In particular, the Office Action states that Huang et al. shows all the elements of the invention recited in claims 1-19 with the exception of a composite gate dielectric layer, which is supplied by the disclosure by Doklan et al., with the combination being viewed as obvious to one of ordinary skill in the art. In addition, the Office Action apparently seeks to combine the prior art references of Huang et al.

and Doklan et al. with that of Yamazaki to provide the element of a thick gate dielectric layer. The rejection is respectfully traversed.

As discussed above with regard to the disclosures by Miyasaka and Yamazaki, the disclosure by Huang et al. calls f or a semiconductor layer that is provided as a single crystalline layer prior to the deposition of a gate dielectric layer (col. 3, lines 6-53). In particular, Huang et al. do not anywhere disclose a rough polysilicon layer upon which a gate dielectric layer is deposited.

Similarly, the disclosure by Doklan et al. fails to teach or suggest the use of a polysilicon layer that is overlaid by a gate dielectric layer. Accordingly, the disclosure by Doklan et al. cannot in fairness be said to teach or suggest the elements of claims 1-19, which include:

> providing a rough polysilicon layer on said insulating substrate;
>
> thermally growing a first gate dielectric layer, in a furnace, on said polysilicon layer;
>
> subsequent to growing said first gate dielectric layer, performing a first anneal procedure to change said polysilicon layer;
>
> thermally depositing a second gate dielectric layer on said first gate dielectric layer; and
>
> performing a second anneal procedure to create a densified second gate dielectric layer, resulting in said composite gate dielectric layer comprised of said densified second gate dielectric on said first gate dielectric layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms,

as is recited in claim 1, and:

> forming a first rough polysilicon layer on said insulating substrate;
>
> thermally growing a first silicon oxide layer, in a furnace, on said polysilicon layer;

subsequent to growing said first silicon oxide layer, performing a first anneal procedure, in situ in said furnace, to improve TFT parametric performance;

thermally depositing a second silicon oxide gate dielectric layer, on underlying, said first silicon oxide dielectric layer, via thermal decomposition of tetraethylorthosilicate (TEOS),

performing a second anneal procedure to densify said second silicon oxide gate dielectric layer, resulting in said composite gate dielectric layer, comprised of densified, said second silicon oxide gate dielectric layer on said first silicon oxide gate insulator layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms;

depositing a second polysilicon layer;

patterning of said second polysilicon layer, and of said composite gate dielectric layer to create a polysilicon gate structure on said composite gate dielectric layer; and

forming a source/drain region in a portion of said first polysilicon layer, not covered by said polysilicon gate structure,

as is recited in claim 7 and:

providing an insulating substrate;

forming a rough polysilicon layer on said insulating substrate;

thermally depositing a silicon oxide gate dielectric layer on said polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700 Angstroms; and

performing an anneal procedure to densify said silicon oxide gate dielectric layer,

as recited in claim 16. Accordingly, the independent claims of the present invention all contain elements that are not taught or suggested in any of the cited prior art references. Namely, each of the independent claims call for a polysilicon layer underlying the gate dielectric layer, whether or

not the gate dielectric layer is a composite or single layer. None of the cited prior art references, either alone or in combination, call for a polysilicon layer upon which a gate dielectric layer is deposited prior to an anneal step. Indeed, each and every reference, with the exception of that by Doklan et al., teach that the semiconductor layer underneath the gate dielectric layer should be a single crystalline silicon layer, which is formed prior to deposition of the gate dielectric layer. The disclosure with regard to Doklan et al. does not teach or suggest anything with regard to the composition of the semiconductor layer underlying the gate dielectric layer.

Accordingly, the present invention recited in claims 1, 7 and 16 recites elements that are not found in any of the cited prior art references, either alone or in combination. Applicants note that the independent claims are amended to recite that the semiconductor layer is a rough polysilicon layer, as is described in the specification on page 6, lines 3-8. In addition, these claims are amended to note that an anneal procedure is performed after a gate dielectric layer is formed on top of polysilicon layer. Applicants respectfully submit that these elements are not shown or suggested in any of the prior art references, and are central to the advantages of the present invention. Accordingly, Applicants respectfully believe that the rejection of claims 1, 7 and 16 under 35 U.S.C. §103(a) is overcome, and respectfully requests that the rejection be reconsidered and withdrawn.

Claims 2-6, 8-15 and 17-19 depend upon and further limit claims 1, 7 and 16, respectively, and should be allowable for all the same reasons as those independent claims, and further because of the additional limitations recited in each of the dependent claims. Accordingly, Applicants respectfully request that the rejection of claims 2-6, 8-15 and 17-19 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Applicants note that the disclosure by Yamazaki is cited for the proposition that a thick gate dielectric layer is formed on a partially polycrystalline silicon layer. However, a review of the pertinent portions of the disclosure by Yamazaki reveals that the reference specifically teaches against the use of polycrystalline silicon. Indeed, in order to obtain the advantages proposed by Yamazaki, the disclosure specifically requires the semiconductor layer under the gate dielectric layer be composed of semiamorphous or amorphous silicon (col. 7, line 18-col. 8, line 3). Indeed, Yamazaki refers to polycrystalline silicon as having a lower carrier mobility than

is required to realize the structure of the patented device (col. 7, line 66-col. 8, line 3). Accordingly, Applicants respectfully submit that the present invention recited in claims 1-19 contain elements that are not taught or suggested by Yamazaki, and indeed are actually opposite to the teachings provided by the disclosure by Yamazaki. Accordingly, allowance of claims 1-19 over the cited prior art references of Miyasaka, Yamazaki, Huang et al. and Doklan et al. is respectfully requested.

Conclusion

Applicants respectfully submit that the foregoing response addresses all issues raised in the most recent Office Action. In addition, in view of the above discussion and amendments, Applicants respectfully believe that the application is now in condition for allowance, and earnestly solicits notice to that effect. If it is believed that an interview would contribute to progress on the application towards allowance, the Examiner is requested to contact the undersigned counsel at the number provided below.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on April 24, 2003:

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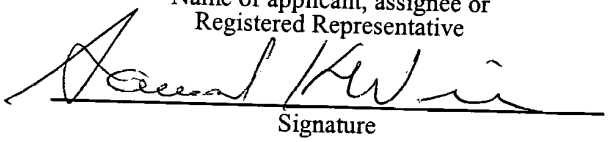
Name of applicant, assignee or Registered Representative



Signature

April 24, 2003
Date of Signature

Respectfully submitted,

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